6 Whittemore Terrace
Wakefield, MA 01880 USA
phone: (781) 245-7825
fax: (781) 246-4548
email: info@analysistech.com

# Electrical Thermal Resistance Measurements for Hybrids and Multi-Chip Packages

**Dr. John W. Sofia**

## ABSTRACT

A discussion of the theory and practice of linear superposition methods for thermal characterization of multi-chip packages and hybrids is presented. A detailed procedure for matrix thermal resistance formulation is described. Test results are presented to demonstrate the method for a multi-chip package. Sources of error and limitations are discussed.

## INTRODUCTION

Thermal resistance characterizations of electronic packages having multiple heat sources are unique and can often pose problems, particularly for the thermal test engineer. Such packages are typified by multi-chip packages or hybrid electronic assemblies. Such devices possess multiple chips often in close proximity. The fundamental effect that differentiates these devices from the single chip packages is that each chip heats the adjacent chips and the relative heat dissipation of the chips may vary depending on the device operation.

Numerical modeling of multiple heat source devices poses no particular difficulty. Predicting the effect of relative variation in the chip heat dissipations can be simply had by making another computer run. The laboratory testing required to verify numerical modeling results is somewhat more difficult for the multiple chip device since multiple chip temperatures need to be sensed simultaneously.

One of the simplest and most accurate methods for measuring chip junction temperatures is the electrical method. This method utilizes an intrinsic property of all semiconductor junctions: a linear relationship between temperature and forward conduction voltage drop at a constant current. This is often called the "$V_{be}$ technique", voltage base-to-emitter, referring to the technique applied to a simple NPN bipolar transistor. A similar technique uses the forward saturation of three-terminal devices. Thus sensing junctions are available on nearly all semiconductor devices and allow the accurate measurement of device junction temperatures using commercially available test systems.

The following discussion covers the method of thermal resistance characterization in multi-chip devices. The underlying theory of linear superposition is briefly discussed followed by the method of thermal resistance matrix formulation. An example with real test data provides comparison of predicted junction temperatures with actual measured values. A simple method for computing a nodal resistance network is detailed. The final discussion covers the physical limitations of the technique.

## METHOD OF LINEAR SUPERPOSITION

The physics of heat transfer is expressed by the general heat-conduction equation and governs the temperature distribution and the conduction heat flow in a solid having uniform physical properties. The Laplace transformation theory that can be used to solve this differential equation includes the superposition theorem, the Duhamel integral theorem, as part of its formalism. The idea of superposition is that known heat conduction solutions for specific heat transfer problems can be superimposed to yield a valid solutions for more complex problems of interest. This principle of linear superposition of heat conduction solutions is an extremely powerful tool which is infrequently applied to thermal testing.

As a simple example of linear superposition, consider the case of a linear conductor bar with internal heat sources, insulated everywhere except at the ends where a fixed temperature is imposed. The temperature distribution within this linear conductor is shown in figure #1 (top) where only a single heat source is operating. With a different heat source operating, a second solution can be easily be generated as shown in figure #2 (middle). Using the method of linear superposition, the solution for the bar with the two heat sources operating simultaneously can be created by simply adding the temperature fields and the heat fluxes. This superimposed solution is shown in figure #3 (bottom) which was created by summing the temperature rises from each single source solution.

The really significant capability offered by this method is that single heat source thermal solutions which are relatively simple to generate, can be superimposed to generate solutions for more complex problems which are relatively difficult to solve by direct approach. The method of superposition can be conveniently expressed through the method of matrix thermal resistance formulations for multiple heat source thermal problems.

## SUPERPOSITION METHOD APPLIED TO THERMAL RESISTANCES

Thermal solutions are often cast in terms of effective thermal resistances in the field of thermal engineering of electronic packages. The method of linear superposition can be applied to thermal resistance characterizations since these are just convenient expressions drawn from more cumbersome full thermal solutions.

Consider the case of the linear bar conduction shown in figures #1, #2, and #3. Physically, this example represents a bar with internally embedded heat sources. The sides of the bar are insulated such that heat can only escape the bar from the uninsulated end faces which are both exposed to an infinite heat sink of temperature $T_0$. The reference temperature for this simple example is the infinite heat sink temperature, i.e., $T_{ref} = T_0$. Superimposing figures #1 and #2, the temperature of point 1 equals the temperature rise of point 1 with only the heat source at point 1 operating plus the temperature rise of point 1 with only the heat source at 2 operating. This is expressed:

$$T_1 = (T_{11} - T_{ref}) + (T_{12} - T_{ref}) + T_{ref}$$
$$T_2 = (T_{21} - T_{ref}) + (T_{22} - T_{ref}) + T_{ref}$$

where the single-source temperatures are :

$T_{11}$ = temperature of pt. 1 with heating from pt. 1
$T_{22}$ = temperature of pt. 2 with heating from pt. 2
$T_{12}$ = temperature of pt. 1 with heating from pt. 2
$T_{21}$ = temperature of pt. 2 with heating from pt. 1

and the superimposed temperatures are :

$T_1$ = temperature of pt.1 due to heat from both pt.1 & pt. 2
$T_2$ = temperature of pt.2 due to heat from both pt.1 & pt. 2

This superposition solution can be similarly expressed in terms of thermal resistances:

$$R_{11} = \frac{(T_{11} - T_0)}{Q_1}$$

where all thermal resistances here are from the heat source "junctions" to the reference temperature, $T_{ref}$ or $T_0$. Here $R_{11}$ is the thermal resistance of point 1 due to heating at point 1. These thermal resistance manipulations can be cast in matrix form for convenience in our case of two heat sources:

$$\begin{bmatrix} \mathbf{R_{11}} & \mathbf{R_{12}} \\ \mathbf{R_{21}} & \mathbf{R_{22}} \end{bmatrix} * \begin{bmatrix} \mathbf{Q_1} \\ \mathbf{Q_2} \end{bmatrix} = \begin{bmatrix} \mathbf{T_1 - T_0} \\ \mathbf{T_2 - T_0} \end{bmatrix}$$

$$[\mathbf{R}] * [\mathbf{Q}] = [\Delta \mathbf{T}]$$

The general thermal resistance description of a device having “N” heat sources is an N-by-N matrix, [R]. The heat dissipation of each source is formed into a column

matrix, [**Q**]. The differences between the source temperatures and the reference also forms a column matrix, [**ΔT**] where with the elements of the array equal to Ti - $T_{ref}$, for i = 1 to N. With the thermal resistance matrix determined, the temperature of each source can be calculated from the above matrix equation based on the principle of superposition.

It should be noted that $R_{12}$ and $R_{21}$ are equal when the selected temperature is an 'independent" temperature. This is to say that the temperature of the reference site should be situated so that it is equally sensitive to the heat fluxes from any of the "junctions" or nodal heat sources and not more sensitive to the heat flux from specific nodal heat source or sources. when this condition is satisfied the [**R**] matrix is a symmetrical matrix. This is a very desirable condition from the perspective of characterizing the device. In regard to the selection of a reference temperature site, an indication of quality is the degree of symmetry of this matrix. This usually means that the local ambient or an average heat sink temperature is the best selection for the reference temperature site. In the case of the local ambient reference site, the local air is not more affected by an particular nodal flux than any other. In the case of the average heat sink temperature, this temperature is ideally influenced by the total heat flux of all of the nodes and not any the heat flux of any particular node. This issue should be considered when selecting the reference temperature site.

## Testing Example

This technique is extremely useful for effective thermal resistance characterization of thermal models on multi-chip modules, hybrids device, or devices having multiple heat sources. It can also be used to verify computer models. The method requires that for each heat source present, one test must be performed. During each test, junction temperatures for all devices must be measured.

This method can be implemented with any junction temperature measurement technique desired although the following demonstration example utilizes the electrical method described above. An Analysis Tech Phase 9 Thermal Analyzer was used to perform the tests. This tester offers simultaneous sensing of multiple junction temperatures. This multi channel capability is essential for packages with multiple internal heat sources. The tester performs automatic computation of thermal resistances.

The test was performed on a hybrid device having five heat sources and thus five junction temperatures. The thermal resistance matrix is a five-by-five matrix. Each row of the matrix required one test with the Phase 9 Thermal Analyzer. In the first test, device 1 was powered while all 5 devices had monitored junction temperatures. The selected reference temperature was the local ambient and thus these resistance values represent junction-to-ambient thermal values. The first test results, rounded to integers, are:

$R_{11}$ = 96°C/watt
$R_{21}$ = 5°C/watt
$R_{31}$ = 3°C/watt
$R_{41}$ = 3°C/watt
$R_{51}$ = 2°C/watt
@ power level of 1.02 watts in device 1

When all five tests have been completed, a total of 25 thermal resistances values have been determined. For this test, the thermal resistance matrix is:

$$[\mathbf{R}] = \begin{bmatrix} 96 & 5 & 3 & 2 & 2 \\ 5 & 86 & 4 & 2 & 2 \\ 3 & 5 & 111 & 9 & 3 \\ 3 & 3 & 10 & 91 & 10 \\ 2 & 2 & 4 & 11 & 95 \end{bmatrix}$$

within the estimated accuracy of the temperature difference measurements of ±1°C, the matrix looks quite symmetrical.

We are now prepared to test the accuracy of the method by powering multiple devices simultaneously and measuring the junction temperatures. By computing the predicted superimposed solution from the above matrix, we can compare these with the actual measured junction temperatures. This test used the following power levels:

| Device Number | Power Dissipation (watts) | Measured Tj (°C) | Predicted Tj (°C) |
|---|---|---|---|
| 1 | 0 | 26 | 28 |
| 2 | 0 | 27 | 29 |
| 3 | 0.5 | 90 | 88 |
| 4 | 0.72 | 105 | 102 |
| 5 | 0.75 | 103 | 105 |

Tref = 24°C

## Computing the Nodal Network

Based on the test results from the above method, a discrete, nodal thermal resistance network can be computed. A requirement for this method is that the [**R**] matrix be symmetrical within the accuracy of the test results. If this matrix is not symmetrical, this method is not valid.

The computation of the network begins the with the [**R**] matrix of dimension N by N (N rows, N columns) that is generated from the matrix superposition method.

Values are then computed for the nodal thermal resistance network interconnecting the N thermal nodes and the reference temperature site. This computation considers each heat source (or junction) as a node in an interconnected network of thermal resistances. Resistors are assigned between each pair of nodes and between each node and the reference temperature site. Figure 4 illustrates this nodal thermal resistance network for a device with N heat sources, i.e., an N node problem.

The designation scheme must be noted for the nodes and the resistances in the network. Each of the N nodes is assigned a number, 1 to N. The nomenclature of the resistors in the network is xij, defined as the nodal resistance connecting node number “i” with node number “j” where i does not equal j; xii where i=j designates the nodal resistance connecting node with the reference temperature site. Thus each node, 'I', has N-1 resistances, xij, j = 1 to N for j <> i, connecting it to each of the other N-1 nodes, and one resistor, Rii connecting it to the reference site. The following discussion deals with the computation of the values of xij and xii starting from the test matrix method test results.

Linear algebra reveals that the nodal resistance network can be described by a matrix [**V**] which is defined:

$$[\mathbf{Q}] = [\mathbf{V}] * [\mathbf{T}]$$

where [**Q**] and [**T**] matrices are the same column matrix of power dissipations and junction temperature, respectively, used above. Based on this definition, the [**V**] is comprised as shown in figure 5. Reproducing the superposition matrix method relationship from above,

$$[\mathbf{T}] = [\mathbf{R}] * [\mathbf{Q}]$$

it is apparent that

$$[\mathbf{V}] = [\mathbf{R}]^{-1}$$

where $[\mathbf{R}]^{-1}$ is the matrix inverse of the [**R**] matrix as defined from the above superposition method. once the matrix inverse has been determined, the values of the N nodal resistances, $x_{ij}$ and $x_{ii}$ can be readily be calculated from the definition of the [**V**] matrix.

## Limitations and Sources of Error

The method of superposition may be used effectively over a wide range of problems. The random errors are always present but these can be quantified by

test repetition and analysis of the sensitivity of the final results to such errors. There are however some situations which may cause significant systematic errors.

1) radiation effects. when radiation becomes a significant means of heat transfer (greater than 5 to 10 % of the total heat transfer) superposition will begin to generate systematic errors. The reason is that the fourth power dependency of radiation is inherently nonlinear and not superimposable.
2) temperature variations in material properties. These are nonlinearities which are not superimposable. To minimize these non-linear effects, all single source tests should be performed at peak temperatures close to those expected in the superimposed solution.
3) certain convection Natural convection generates a non-superimposable non-linearity since the convective action depends on the total amount of heat dissipated leading to buoyancy. Down stream convection effects where components are down stream of heated components will be heated by fluid warmed by up-stream components must use the local air temperature. Fluid dynamics effects are generally non-linear and thus can create systematic errors for superposition method.

## APPLICATION TO REAL TESTING

A typical application of the above technique would be for verification of thermal models on multi-chip modules, hybrids device, or devices having multiple heat sources. For each heat source present, one test must be performed. During each test, junction temperatures in all devices must be measured.

## CONCLUSION

The method of linear superposition offers an effective means for dividing a difficult thermal characterization problem into simpler problems that can then be combined to reach the complete solution. This benefit is particularly useful for multi-chip test characterizations.

Figure 1

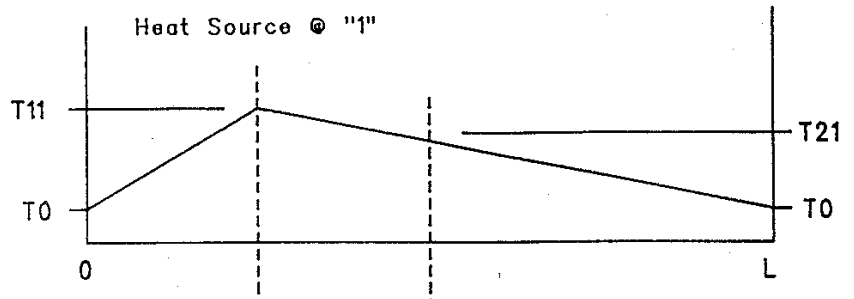



Figure 2

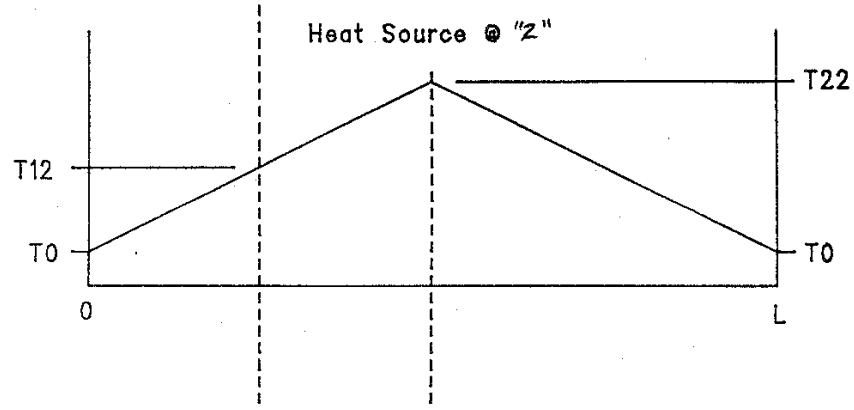
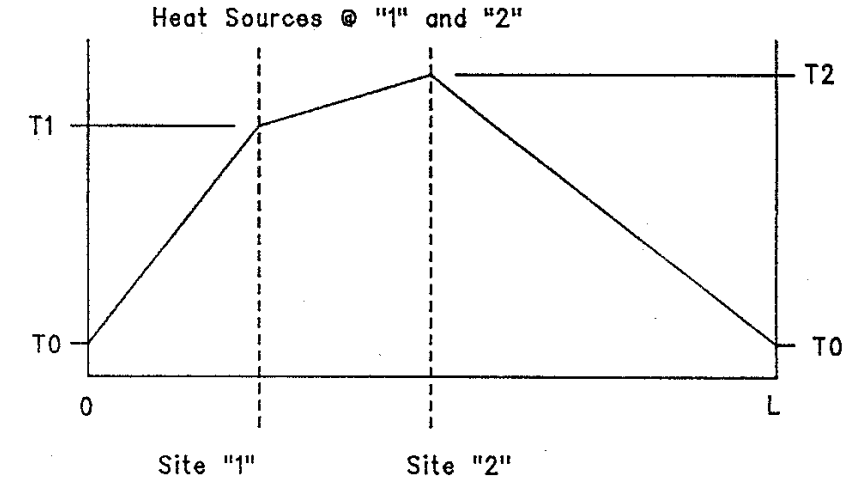



Figure 3




Temperature profiles for point-heat-sources in an insulated bar of length 'L' with ends at fixed temperature, T0

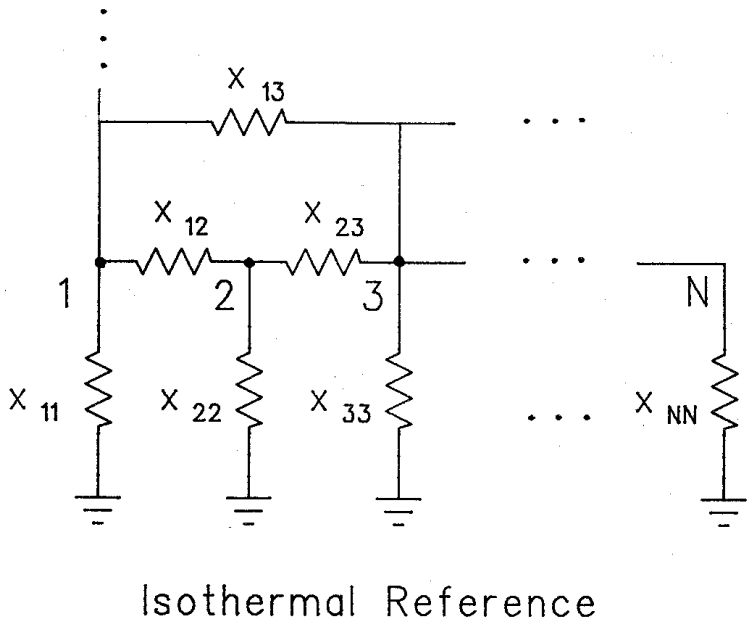



**Figure 4: Illustration of nodal resistance network concept and nomenclature**

$$\begin{bmatrix} \sum_{i=1}^{N} X_{1i}^{-1} & -X_{12}^{-1} & -X_{13}^{-1} & \cdots & -X_{1N}^{-1} \\ -X_{21}^{-1} & \sum_{i=1}^{N} X_{2i}^{-1} & -X_{23}^{-1} & \cdots & -X_{2N}^{-1} \\ -X_{31}^{-1} & -X_{32}^{-1} & \sum_{i=1}^{N} X_{3i}^{-1} & \cdots & -X_{3N}^{-1} \\ \vdots & \vdots & \vdots & & \vdots \\ -X_{N1}^{-1} & -X_{N2}^{-1} & -X_{N3}^{-1} & \cdots & \sum_{i=1}^{N} X_{Ni}^{-1} \end{bmatrix} = [V]$$

**Figure 5: Composition of [V] matrix for computation of discrete nodal resistances**