# Analysis of Thermal Transient Data with Synthesized Dynamic Models for Semiconductor Devices

Dr. John W. Sofia, Analysis Tech, Wakefield, MA 01880

*Abstract*—**A technique for synthesizing dynamic models comprised of discrete thermal resistances and capacitances directly from thermal step-response data on packaged semiconductor devices has been developed. Such models reveal the effective internal-package thermal resistances which comprise the overall junction-to-ambient or junction-to-case thermal resistance. These models can discriminate lumped internal constituent resistances including die/die-attachment spreading, internal package spreading, and case-to-air dissipation. The thermal step-response has been experimentally and analytically studied using the electrical method of junction temperature measurement. The interpretation and accuracy of these synthetic models have been investigated on a collection of test-case devices. Overshoot anomalies exhibited by junction-to-case thermal step responses have been examined experimentally and explained with synthetic model analysis. The application of synthetic models to computing thermal impedance for non-constant or cyclic device-powering conditions is also presented.**

## Introduction

This research began with the hypothesis that simple mathematical models could be used to simulate the transient thermal behavior of semiconductor devices and provide an aid to interpreting thermal step-response data. The thermal step-response, traditionally known as "transient response" or "heating curve", measures the junction temperature after an abrupt step-change in internal power dissipation. Junction temperature measurement is accomplished using the well-established method based on temperature-dependent electrical parameters. [1, 2] As the step-change in power heats the device from an initially unpowered equilibrium condition to powered, steady state equilibrium, the resulting thermal data stream embodies the transient and equilibrium thermal characteristics of the device-under-test. This step response data is often termed "heating curve data" since the data plot details the heating of device. Previous analysis of the thermal step-response has been primarily limited to graphical interpretation of the "heating curve".

A technique for synthesizing dynamic models comprised of discrete thermal resistances and capacitances has been developed for improved physical insight. These models provide three significant benefits:

1) delineation of effective internal package thermal resistances and time constants.
2) delineation of the best "target" for package thermal enhancement efforts and estimate of probable results.
3) simulation of the behavior of the device to non-steady or cyclic powering conditions.

The use of thermal step-response has historically been limited to the measurement of junction-to-ambient thermal impedances. When dealing with devices which are designed for heat sink attachment, the junction-to-ambient impedances are not useful for general characterization. For this reason, the thermal step-response has been applied to the measurement of junction-to-case thermal impedances. Anomalies in the junction-to-case step-response have been observed for certain devices. An explanation for these anomalies is offered with synthetic models. A workable approach for dealing with the step-response data from devices which exhibit these anomalies has been developed and demonstrated.

## Step Response and Synthetic Models

The analysis of transient dynamics in electrical and mechanical systems frequently utilizes the step-response technique. Here, an instantaneous step-change in system inputs or disturbances is used to reveal the behavior of the physical system. The wide spectral content of the "step" broadly stimulates the system as it changes state from one equilibrium condition to another in response to the perturbation of the step. The transition between pre-step and post-step equilibrium conditions contains all of the information needed to synthesize a dynamic model capable of simulating or predicting the response of the linear physical system to any disturbance or operating condition. Such models can also provide physical insight into the internal composition of the system. Throughout this work, it is assumed that we are dealing exclusively with linear systems or systems that are sufficiently linear over the operating range of interest.

Figure 1 illustrates an example of mock empirical data for the step response of a mechanical system. This plot expresses position versus time after a step in mass-loading occurred at time zero with the system previously in static equilibrium. A generic, hypothetical model (figure 2) consisting of a mass, spring, and damper exhibits similar dynamics and thus could potentially mimic (model) the empirical data from the physical system. Optimum values for the model mass, spring constant, and damper coefficient can be assigned so that the computed (simulated) response of the hypothetical model best matches the empirical data. The process of selecting a candidate model and the assignment of optimum values for its parameters based on the empirical data is called synthesis and the result is a synthetic dynamic model. [3] This synthetic model can offer insight into the composition and behavior of the system.

The candidate model provides a template with a specified number of assignable parameters. In the previous mechanical system example, there are three parameters consisting of idealized, discrete physical components. Candidate models are often comprised of more complex mathematical functions which do not offer such intuitive insight. Such models can be stated in frequency or time domains and are not generally amicable to simple physical interpretation. Standard techniques for model synthesis based on discrete Fourier transforms and Z-transforms are available [4] and can be applied to the analysis of thermal step-response of packaged semi-conductors.

The technical literature offers many other techniques which evolved to handle specific types of synthesis problems. Although some of these existing techniques have been applied as part of this work, a superior technique has been developed which utilizes a simple resistor-capacitor candidate model, shown in figure 3. Presentation of the mathematical techniques involved in dynamic model synthesis is beyond the scope of this paper.

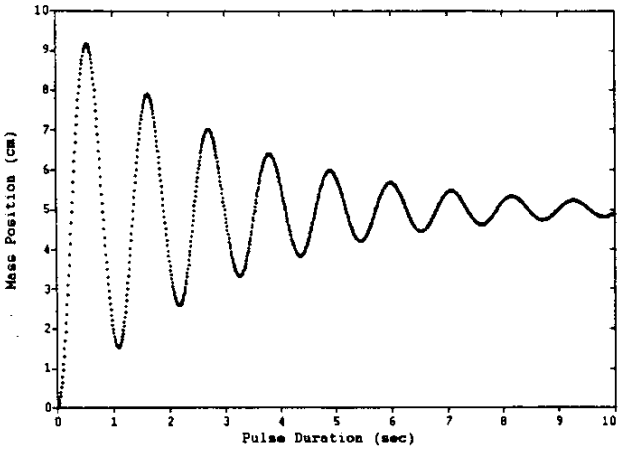


Fig. 1. Mock empirical data from hypothetical mechanical system

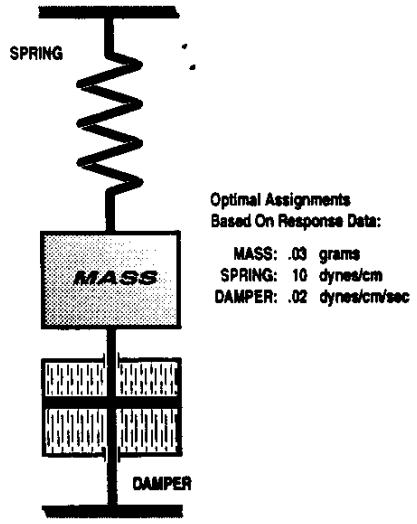


Fig. 2. Candidate model for mechanical system example

The candidate model of figure 3 suggests an idealized discrete network representing the packaged semiconductor. The resistances represent a lumped version of the distributed three-dimensional thermal resistance network of the package, from die to ambient. The capacitances represent the lumped three-dimensional distribution of heat capacitance. The upper node is the heat dissipating junction, the bottom node, the local ambient. The intermediate nodes represent unspecified boundaries within the package, the location of which may vary somewhat over the duration of the heating-step. Although it will be shown that approximate locations for the intermediate node boundaries can be inferred from the synthesized model, the physical location of these nodes is not specified or fixed by the model synthesis.

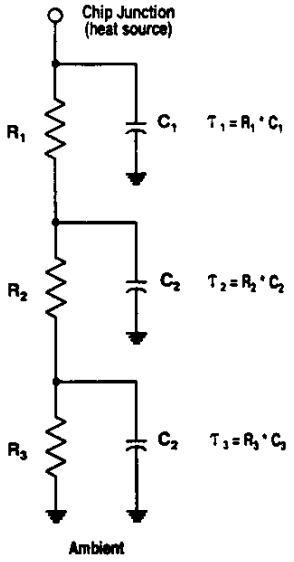


Fig. 3. Candidate model of three discrete thermal resistor/capacitor pairs (third order model)

The candidate model of figure 3 uses 6 independent, orthogonal variables: 3 resistors and 3 capacitances. Often the model is expressed in terms of resistors and time constants (Ts) although it should be noted that there are no longer 6 orthogonal variables. Since each of the 3 time constants are the product of their associated resistances and capacitances, changing a model resistor also changes its associated time constant. Although both time constant and heat capacitance expressions of the synthetic model provide unique advantages, the use of time constants often provides somewhat more insight than heat capacitances despite the loss of orthogonality.

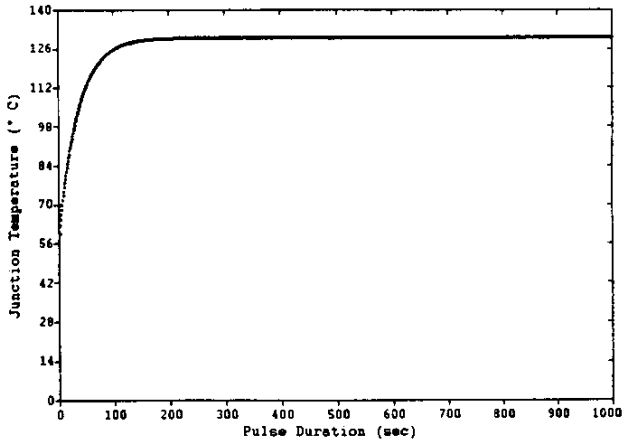


Fig. 4. Modeled step-response plotted using junction temperature versus linear time

Figure 4 plots the junction temperature of a hypothetical packaged semiconductor in response to a step change in power dissipation. The X-axis is a linear time axis where zero is the instant of step-initiation and the Y-axis is the junction temperature. This selection of plot axes is not well suited to present the data since the step-heating response is characterized by changes that are initially very fast followed by

successively slower rates of change in the junction temperature. The same data is presented in figure 5 where the X-axis uses log-time. When plotted in this manner, the data curve exhibits plateaus or ripples which are associated with the internal thermal capacitances and resistances of the package. For these reasons, the log-time plot is universally accepted for thermal step-heating curves.

The heating step-response curve of figure 5 illustrates typical characteristics worth noting. The variations in slope with shallow "plateaus" are a common manifestation. This plot is the result of a model synthesis based on the candidate model of figure 3 with the assigned model parameters indicated on the figure 6 plot. Each section or "stage" of the model has a time constant, $\tau$, which equals the product of the thermal resistor/capacitor pair for that stage of the synthetic model. Recalling that an exponential function exceeds 95% of its final value after 3 exponential time constants have elapsed, figure 6 reveals that each of the points of inflection correspond to approximately triple one of the time constants in the synthetic model. Thus, each ripple in the heating step-response indicates an equilibrium condition of a particular intermediate stage of the model with respect the next slower (larger $\tau$) stage of the model. The final plateau is reached when all three stages of the model near thermal equilibrium on the extreme right of the plot

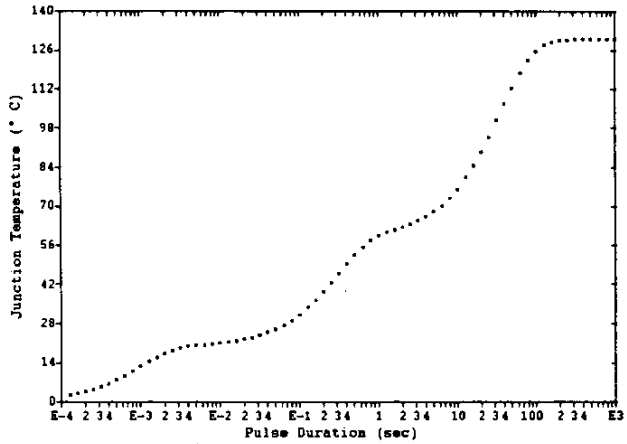


Fig. 5. Modeled step-response plotted using junction temperature versus log-time

The heating step-response can be considered a cross sectional view of the internal thermal resistance of a device as depicted in figure 6. The following mechanistic description will help demonstrate this fact: Shortly after the instant of step-transition, heat is flowing through the die and is beginning to enter the die attachment region. The small heat capacitance of the die region permits a significant increase in the die temperature with only a small accumulation of heat energy. Thus initial temperature rises are almost entirely governed by thermal spreading in the die region. The mass of the package, with its larger heat capacitance, will respond later, after sufficient energy accumulation required to alter its temperature. In general, the larger the heat capacitance associated with a thermal resistance, the longer the heating interval until its influence will be manifested. Step-response plots depict internal thermal resistance versus distance from the die and thus effectively a thermal resistance cross section of the device, given the overall spreading character of package heat flow.

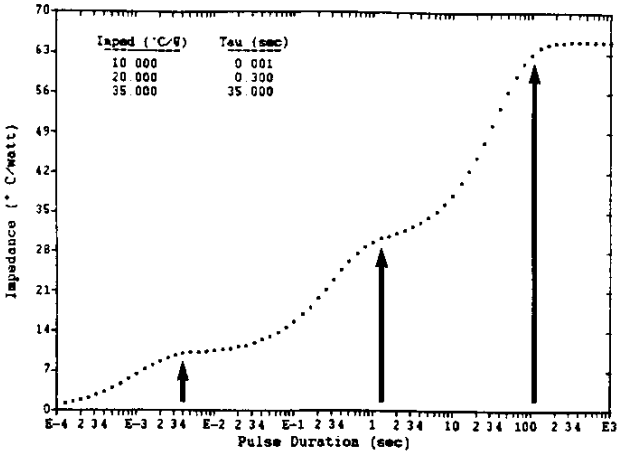


Fig. 6. Modeled step-response plotted using impedance versus log-time

Figure 6 uses thermal impedance rather than junction temperature for the ordinate as in figure 5. It should be noted that thermal impedance is defined as non-equilibrium thermal resistance so that thermal impedance equals thermal resistance at equilibrium. Generally, thermal impedance offers a superior expression of step response data over junction temperature since the statement of power is implicitly included. It should also be noted that the sum of the constituent thermal resistances equals the steady state thermal resistance of the package.

## Selected Test Cases

To demonstrate the capabilities and characteristics of synthetic model analysis, the results of two test cases are discussed. These sample test cases demonstrate the analytical capabilities of synthetic model analysis.

### Plastic and Ceramic IC Package Test Case

Figure 7 presents data for a step-response test on a 24 pin DIP plastic package mounted on a test-PWB in still air. Figure 8 presents data for the identical test performed on a ceramic package, cavity up, with an identical die. Each plot consists of the original test data (small data points) overlaid with the synthetic model simulation data (larger points). The excellent agreement between the test data and the model is apparent. The model parameter assignments are expressed in constituent impedances (°C / watt) and time constants ($\tau$, in seconds) on each plot. Each model utilizes widely spaced time constants, nearly two orders of magnitude separated, indicating a high degree of model-uniqueness.

The thermal impedance that is paired with the shortest time constant is associated with the lumped thermal resistance nearest the die, including at least the die and die-attachment. Extending this concept to other components of the model, Figure 9 compares the test data of figures 7 and 8. It must be emphasized that the boundaries of the die, package, and environment as construed by the synthetic model are

not constrained to the typical definitions. Thus the boundary of the die-region-spreading may include a portion of the package directly adjacent to the die-attachment; the outer boundary of "case-spreading" may be inside the package. In addition, it is anticipated that these imaginary boundaries probably change somewhat during the heating-step; therefore the concept of precise boundary location has little merit or validity.

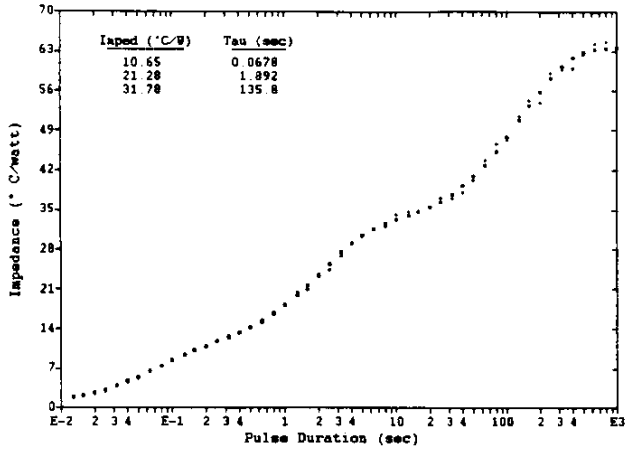


Fig. 7. Response of plastic 24 lead DIP

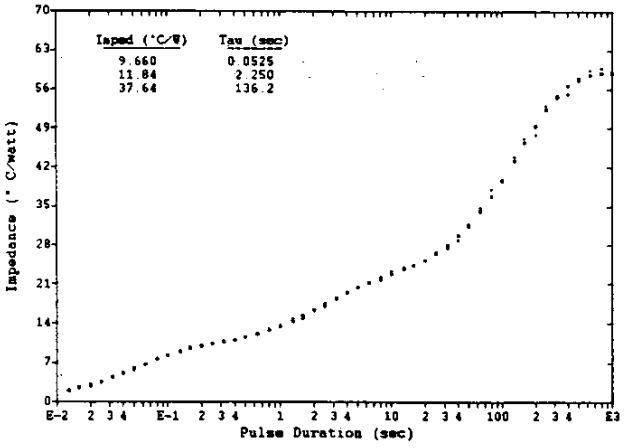


Fig. 8. Response of ceramic 24 lead DIP

With the help of figure 9, it is clear that both plastic and ceramic packages possess nearly equal die-region-spreading thermal resistances, a result of the fact that the same die was used in both packages. The case-spreading component shows the plastic package to be far more resistive than the ceramic package by nearly a two-fold difference. This is almost certainly due to the difference in material conductivity and geometry of plastic versus ceramic packages. The case-to-ambient thermal resistance component is about 15% higher than that of the ceramic package. This could be due to the conduction geometry of the cavity in the ceramic or the presence of the copper lead frame of the plastic package acting as a heat spreader to ambient which would be manifested in the case-to-ambient constituent resistance.

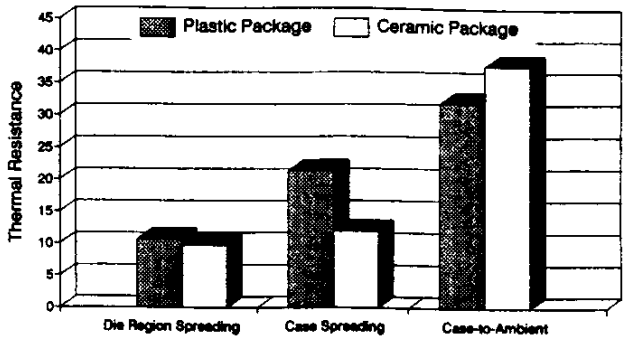


Fig. 9. Comparison of constituent thermal resistances for plastic and ceramic 24 DIP packages

Figure 9 also indicates that the largest component of the junction-to-case thermal resistance is the case-to-ambient thermal resistance with the die spreading and case spreading together comprising only 50% of the case-to-ambient thermal resistance. Clearly significant improvements in the junction-to-ambient thermal resistance of the ceramic package are possible by improving the case-to-ambient resistance. This is far less true for the plastic package based on a similar consideration. In this manner, the comparison of the relative magnitudes of the constituent thermal resistances provides insight for package enhancement engineering.

Comparing the model heat capacitances with estimated values for the device can provide insight into the physical boundaries represented by the intermediate nodes of the model. Heat capacitances can easily be computed from the model for the ceramic package test data of figure 8. Using a very simplistic approach, the package will be assumed to be comprised of the die, cavity floor, and remainder of the package. The die-region model heat capacitance is 0.0054 J/°C versus 0.0051 J/°C for the actual die (assuming a heat capacitance for silicon of 1.66 J/°C/cc). The model "package spreading" heat capacitance of 0.19 J/°C compares to the heat capacitance of the "floor" of the cavity equaling 0.30 J/°C (assuming a heat capacitance for ceramic of 3.35 J/°C/cc). The longest model time constant yields an associated heat capacitance of 3.6 J/°C versus 3.8 J/°C of the entire body of the ceramic package excluding the cavity and its "floor" as well as the leads. Figure 10 presents the comparison between the model heat capacitances and the estimated heat capacitances based on our assumed segmentation of the package into die, "floor" and "remainder".

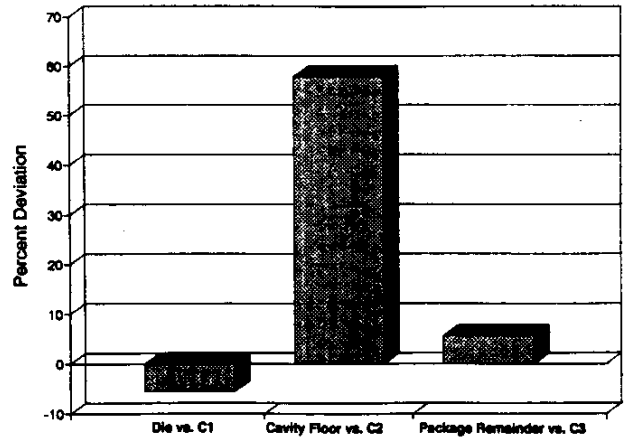


Fig. 10. Comparison of constituent heat capacitances with estimated heat capacities of package

This comparison suggests that the model die region node boundary correlates quite well with the physical die with less than 6% discrepancy in modeled versus computed heat capacitances. The model "package spreading" heat capacitance shows a relative poor agreement to the "floor" heat capacitance with a 58% difference. This large discrepancy suggests that not all of the "floor" is included within the model "package spreading" boundaries. The package "remainder" heat capacitance shows good correlation to the model "environment" heat capacitance. Clearly, the assumed boundaries for estimating the heat capacitances were somewhat arbitrary. Even where good agreement between model and estimated values exits, the assumed boundaries may be quite imprecise. It should also be noted that the concept of fixed, precisely located boundaries is probably false. Rather, evidence suggests that the boundaries are "shaded" transition regions. This heat capacitance comparison provides some insight into the boundaries of the constituent thermal resistances.

## Copper Slug IC package

Figure 11 presents step-response data with an overlaid synthetic model simulation for a copper slug IC 168 lead quad package. The synthetic model for this package uses only two resistor/capacitor pairs, ie., a second order model. When a model synthesis utilizing the standard third order model (figure 3) is attempted, the synthesis degenerates into a second order model. Mathematically, this occurs when the optimization yields one of these conditions,

a) a time constant much larger than the duration of the step-response test,
b) a resistor or heat capacitance which is insignificantly small,
c) two time constants which are different by less than a multiple of 2 or 3

Physically this occurs when the candidate model contains more lumped time constants than are needed to model the data. Reducing the order of the model corrects this situation. In this case, the test data in figure 11 is well suited to the second order synthetic model as evidenced by the nearly coincident overlaid curves.

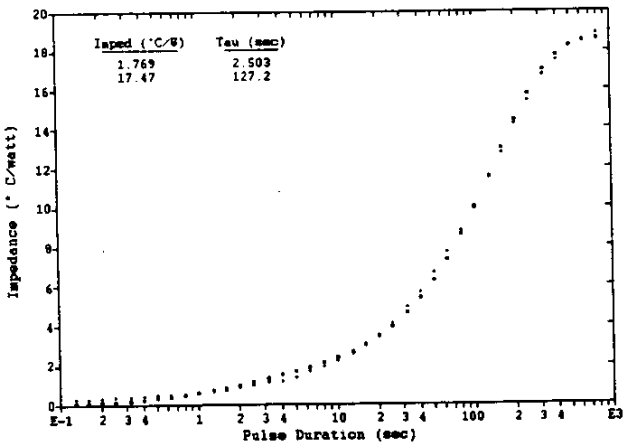


Fig. 11. Response for 208 lead copper slug package

Figure 12 presents the data and model simulation for the same copper slug package but with a failed die-attachment. Here the synthetic model does not degenerate into a second order model. Clearly, the failed die-attachment introduces a third, distinct, constituent thermal resistance. Limiting the candidate model to second order and resynthesizing the model yields the plot of figure 13. A comparison of the test data curve with the model simulation curve indicates that although the second order model is a reasonably good match, the previous third order model was better.

Forcing the second order fit permits the comparison of constituent thermal resistances in figure 14. The die-region constituent thermal resistance is about four times higher for the device with the failed die attachment. There is good agreement between the case-to-ambient constituent thermal resistances.

Figure 15 compares two tests performed on the previously tested device with the failed die attach at different power levels. The test with 30% less power exhibits a 20% higher case-to-ambient constituent resistance. This effect is most probably due to the mechanism which drives the natural convection cooling of the device. Due to the reduced amount of heat rejected into the local ambient, the buoyancy-driven natural convection plume will be less intense and therefore provide lower convective heat transfer and higher convective thermal resistance.

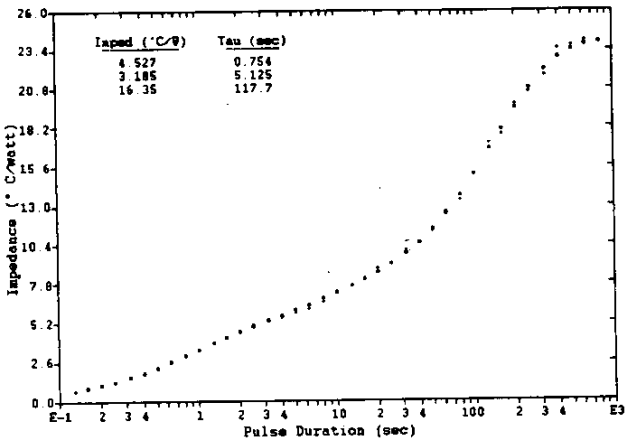


Fig. 12. Response for slug package with failed die attachment, third order model

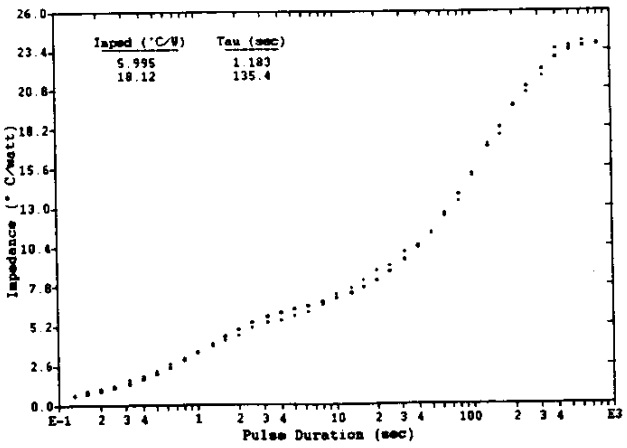


Fig. 13. Response for slug package with failed die attachment, second order model

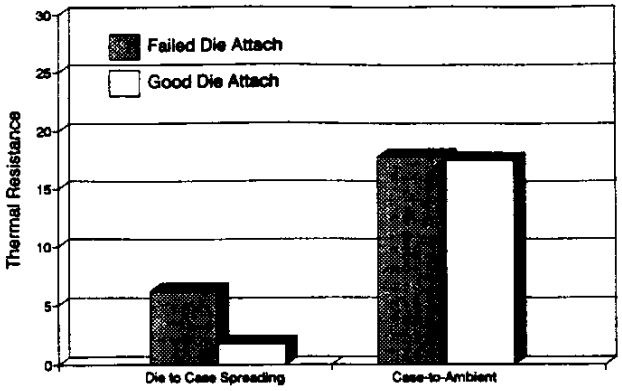


Fig. 14. Comparison of model constituent resistances for good and failed die attachments

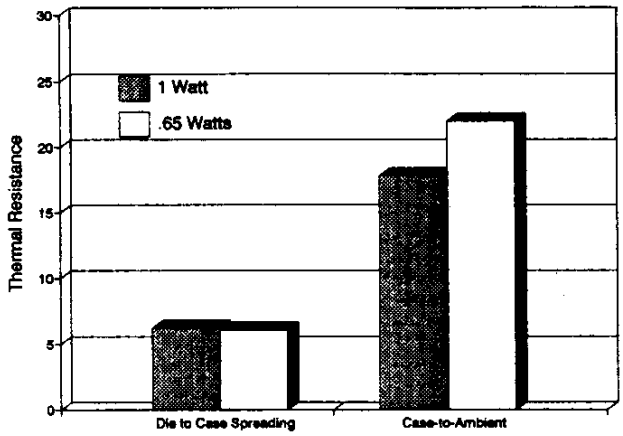


Fig. 15. Comparison of model constituent resistances at two power levels of heating step

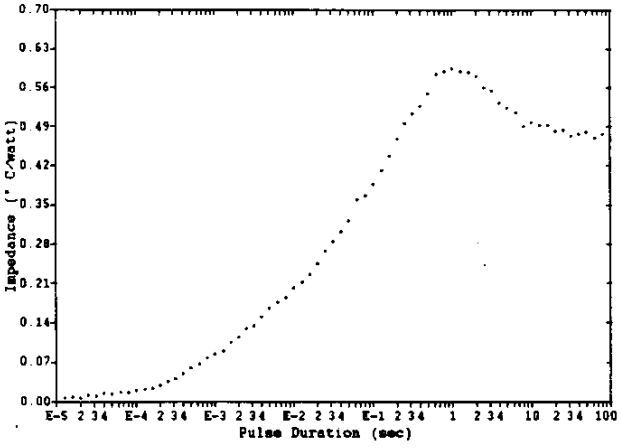


Fig. 16. Junction-to-case thermal step-response; thermocouple under tab

Examining the model constituent heat capacitances, the good die attachment (fig. 11) yields 1.4 and 7.3 J/°C; the bad die attachment (fig. 13) yields 0.2 and 7.5 J/°C. The large difference between die region heat capacitances is noteworthy. Clearly the actual die has the same heat capacitance in both devices;the difference in the model capacitances suggests that much more than the die is included within the die region boundaries of the device with the good die attachment. It also suggests that the node boundaries are quite different for the "good" versus the "failed" device in the die region. The agreement for the outer package heat capacitances is good. Examining the package construction details, the integral copper slug contributes less thanhalf of the model outer package heat capacitance based on an estimated slug heat capacitance of 3.1 J/°C. Clearly the model boundaries of the outer package include much more than just the copper slug although the complex internal geometry of materials preclude a simple estimation of the heat capacitance of the package as a whole.

## Junction-to-Case Measurements

Packages such as the TO-220, TO-247, TO-202, and other styles with integral heat-tabs are designed for heat sink attachment. Junc-

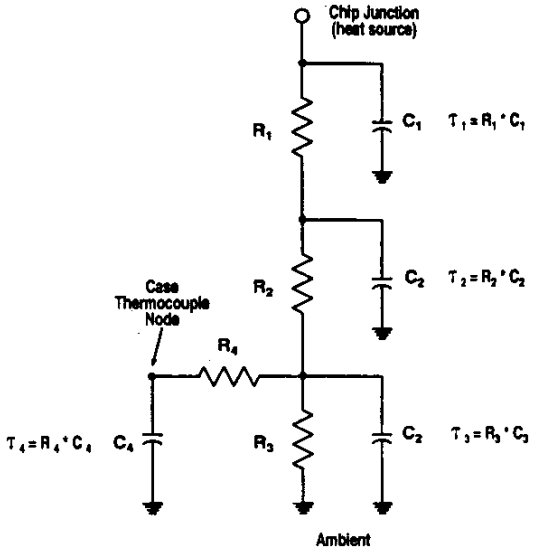


Fig. 17. Candidate model for junction-to-case simulation

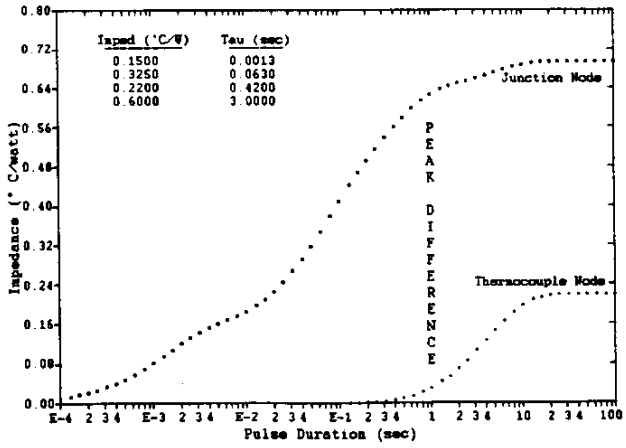


Fig. 18. Simulated response of junction node and thermocouple node model of data from Fig. 16

tion-to-case thermal resistance measurements are required for meaningful thermal characterization of such packages. The designated site for the case temperature measurement is usually either at the root of the center lead on three lead devices or directly under the die on the face of the tab in contact with the heat sink.

Figure 16 presents junction-to-case step-response test data for a (MTP20N20E, MOSFET) TO-247 device with the case temperature measured under the die. The anomalous "bump" or "overshoot" exhibited is commonly observed in tests of this type. The bump suggests that the thermal resistance is highest for some particular heating duration, after which, continued heating yields significantly decreased thermal impedance. Physically, this does not seem possible. The plot indicates that the steady-state junction-to-case thermal resistance is significantly less than the peak thermal resistance.

Figure 17 presents the candidate synthetic model for junction-to-case measurement. This model differs from our previous model of figure 3 by the presence of the thermocouple node with its associated heat capacitance and interconnecting resistor. The rationale behind this modified model is that the selected thermocouple site most probably does not the correspond to one of the intermediate node boundaries of the model and must be therefore interconnected with a lumped resistance and capacitance. Although more complex candidate models could be devised, this one is the simplest one that exhibits the required step-response characteristics. Figure 18 plots the junction-to-ambient and the thermocouple-to-ambient step responses together. The difference between these two curves yields the junction-to-thermocouple curve of figure 19. Note that the difference between these two curves exhibits an overshoot caused by the difference in response time of the thermocouple node with respect to the junction node. Thus the anomalous "bump" is an artifact of the phase difference between the thermocouple node and its adjacent node.

Figure 19 presents the synthetic model performance overlaid with the data of figure 16. (This model synthesis is less tightly performed due to the approximate algorithm utilized.) Clearly, this synthetic model accounts for the anomalous test data. If the part is retested using the root of the center lead as the case temperature site instead, the bump artifact becomes significantly larger as shown in figure 20. The size of the bump also varies dramatically depending on the part type. Some device types in the TO-247 package exhibit little or no bump when the case temperature is measured under the die but a significant bump when the root lead site is used; some devices do not exhibit a bump for either case temperature site. This suggests that variations in the size of the overshoot are due to differences in the thermal resistance between the case thermocouple and its adjacent node boundary as well as the device-specific network internal thermal resistances. In other words, the closer the thermocouple lies to the nodal boundaries, the smaller the overshoot.

The synthetic model for junction-to-case measurements effectively accounts for the anomalous bump. The physical insight imparted by the model also suggests an effective approach to analyzing the data. Based on the model, the bump anomaly is caused by the phase (timing) difference between the case thermocouple node and the junction node. This artifact has no significance for predicting the thermal performance of the device since it would only result in artificially higher estimated junction temperatures based on the measured case temperature. Based on this, the bump anomaly can be handled by simply truncating the bump where it exceeds the steady state thermal resistance. Applying this principle, the synthetic model simulation is overlaid on the data of figure 16 and shown in figure 21. In this case, only a two stage model is needed reflecting the simple thermal network and few sensible resistance interfaces between the junction and the case-thermocouple.

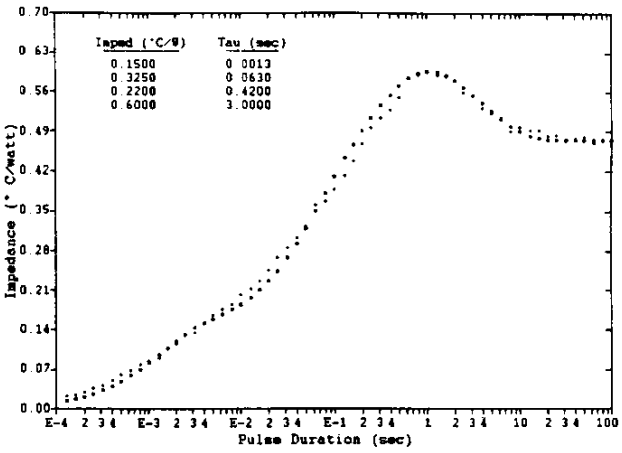


Fig. 19. Model simulation overlaid on data

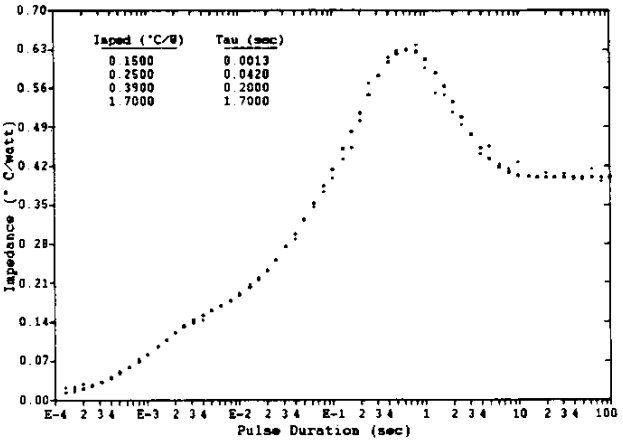


Fig. 20. Step response with case thermocouple on root of center lead

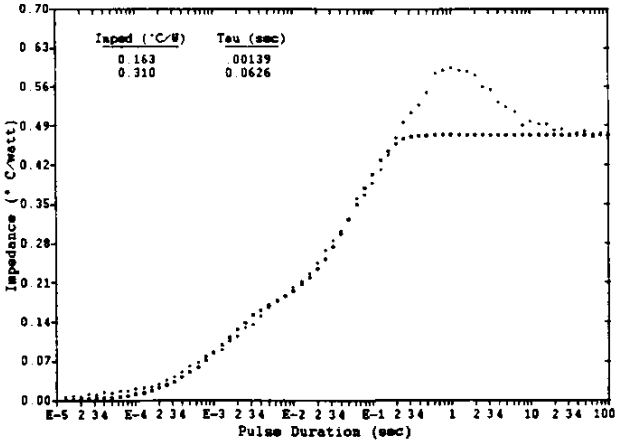


Fig. 21. Response of model which excludes the anomalous bump

## Uniqueness and Tolerance of Synthetic Models

The uniqueness of a synthetic model is intimately associated with the tolerance that can be attributed to the model parameter assignments. The uniqueness of a synthetic model is defined as the degree to which variations in parameters in one stage can be compensated by adjustments in other stages. Uniqueness can also be considered the "sharpness" or criticality of the optimum parameter assignments. A sharply defined optimum model becomes significantly non-optimal for small variations in any of the model parameters and variations of one model parameter cannot be compensated by adjustment in other model parameters. Conversely, a "broad" optimum permits compensation for one parameter adjustment by the other parameters with minimal change in the degree of optimality. The sharper the optimum, the higher the model uniqueness.

The primary indicators of model uniqueness are the proximity of the time constants (expressed as multiples) and the quality of the match between the actual test data the model simulation. The more wide-spread the $\tau$s, the more unique the model. Uniqueness starts to become a concern for multiples less than 10. Generally, multiples between adjacent $\tau$s greater than five are desirable and models with time constants which are different by less than a multiple of 2 or 3 are degenerate and suggest a synthetic model with 1 less resistor/capacitor pair. Regarding the quality of match between the data and the model simulation, it is clear that the worse the agreement, the less unique the model.

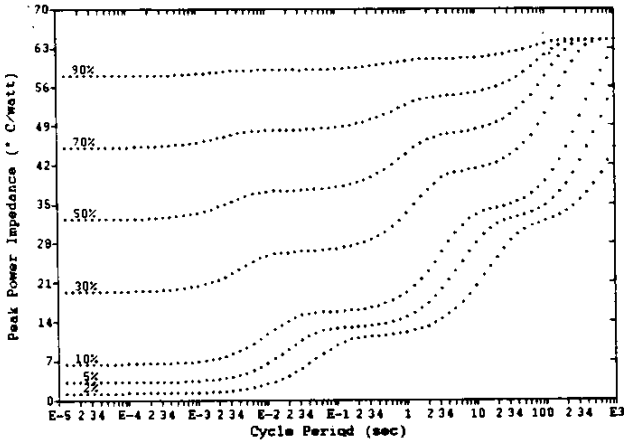


Fig. 22. Impedance simulation for square waves of various frequency (period) and duty cycle based on synthetic model

## Simulation of Non-Uniform Power Conditions

The synthetic dynamic model for a device can be used to simulate the thermal performance in response to power conditions other than the simple step. Arbitrary power waveforms can be specified as the input to the synthetic model. The resulting simulation can completely detail the thermal performance of the device. Typical power waveforms include square-wave power inputs of varying duty cycle although any arbitrary waveform can be used. An example of such a plot is provided in figure 22 based on the model of figure 6. These curves correspond to a range of different duty cycles expressed in percent, labeled on each curve. Arbitrary wave forms can be utilized when specified in step-wise approximation.

## Conclusion

Synthetic dynamic thermal models derived from step-response test data on packaged semiconductors offer impressive potential for measuring the effective internal thermal resistances of packages. Such models essentially offer a cross sectional view of the effective internal resistance elements comprising the overall thermal resistance of the package. Analysis of the model constituent heat capacitances can suggest approximate, physical node boundaries. The interpretative capability of synthetic dynamic models offers invaluable potential for guiding package thermal enhancement.

## Test Equipment Description

The thermal test data and synthetic models for this research were generated using Analysis Tech Thermal Analyzers, Phase 7 and Phase 9 models. This research was conducted at the Analysis Tech semiconductor thermal laboratories, Wakefield, Massachusetts. Candidate models incorporating the thermocouple node for case temperature were synthesized using non-standard, custom "soft" algorithms with "looser" optimization capability. Additional questions on this research should be directed to Dr. John W. Sofia, Analysis Tech, (617)-245-7825 or FAX: (617)-246-4546.

## References


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