Investigation of Solder Fatigue Acceleration Factors

L. R. FOX, J. W. SOFIA, AND M. C. SHINE

Abstract—**Solder fatigue was investigated experimentally for effects of the strain loading waveform in isothermal mechanical fatigue, and frequency and strain range in true thermal cycling. Rapid strain loading followed by a long hold period at constant strain was found to be very damaging compared to constant rate cycling at the same peak amplitude and period. Thermal cycle fatigue data showed a stronger dependence on cycle period and weaker dependence on strain range than reported results in isothermal mechanical fatigue. Implications of the experimental findings are discussed with regard to solder joint fatigue and accelerated life testing of leaded chip carriers. Isothermal mechanical fatigue testing was carried out at room temperature with a custom torsional apparatus having an optical servo-loop for strain control. Mean joint compliance change per cycle was used as a fatigue metric. Experiments were carried out on 5/95 and 63/37 Sn/Pb solder joints. Mean stress in the solder joints was measured at 23°C and found to relax significantly after several minutes. Thermal cycle experiments were carried out with an air impingement apparatus capable of cycling the test samples between 30–110°C in periods ranging from 2 to 120 min. Ceramic chip carriers were soldered to aluminum, zinc, and stainless steel substrates to permit fatigue life data to be taken from 0.3–14 percent strain range. A conventional crack criterion was used as the fatigue metric in the thermal cycle experiments. A simple finite element model of a 68 post molded leaded chip carrier (PLCC) was analyzed to examine expected stress loading of the solder joints under typical operating conditions. Transient thermal stress loading and low stress creep of the solder joint are discussed in light of this model and known creep properties of solder. It is shown that during typical operating cycles, the total creep strain can account for the majority of plastic or nonrecoverable strain.**

INTRODUCTION

Scope

THE EMERGENCE of commercially viable surface mount module technology has focused considerable interest on the problem of solder joint fatigue in thermal cycling. The operating environment of commercial computers typically imposes cyclic thermal stress–strain loading on component solder joints due to power dissipation. Fatigue damage in solder is known to result from repeated thermal cycling, and has received much discussion [1], [2]. Although solder fatigue problems in leadless chip carrier systems have received the bulk of attention, solder joint strains will also be present in the leaded carrier. Thermal deformations following rapid power on/off transients (minutes) will store elastic energy in the compliant lead which can then drive creep strains in the solder joint for long times (hours). Since creep rate and stress relaxation are stress and temperature dependent, care must be exercised in choosing an appropriate method for accelerated joint life testing in these systems. Much data for fatigue life estimation remains to be generated, particularly for low strain range thermal fatigue cycling.

This paper presents some experimental results on solder fatigue concerning the effects of strain rate loading in isothermal mechanical fatigue, and on frequency and strain range variation in true thermal cycling. Rapid strain loading followed by a long hold period at constant strain was found to be very damaging compared to constant rate cycling at the same peak amplitude and period. Thermal cycle data showed a stronger dependence on cycle period and weaker dependence on strain range than reported results in isothermal mechanical fatigue. The mean change of joint compliance per cycle was used as the fatigue criterion in the isothermal mechanical fatigue tests, and found to correlate well with other observations. This method of testing is convenient in that fatigue to ultimate fracture need not be carried out in all cases, thus shortening test time in long running low strain experiments.

Stress–Strain Loading for Leaded Carrier

A simple finite element wedge model for periodic boundary conditions was used to analyze solder joint stress in a typical surface mounted plastic post molded leaded chip carrier (PLCC) with 68 leads (Fig. 1(a)). The carrier was assumed to be at the center of a section of FR-4 PWB 32 mm (1.25 inch) square with adiabatic edges. Nominal operating conditions were assumed: power dissipation 1 W, moderate forced convection at 2 m/s (400 FPM). Degraded airflow was assumed between the carrier and the board, and on the board bottom, with the following values of convective heat transfer coefficient H (mW/cm^2): carrier top and leads $H = 2.4$; carrier bottom, PWB top (included under carrier) $H = 0.8$; PWB bottom $H = 1.6$. A copper alloy leadframe with J-bend external lead was assumed, having overall height (foot to shoulder) 2.5 mm (0.095 inch), width 0.71 mm (0.028 inch), and thickness 0.25 mm (0.010 inch). To further simplify the model, an angular form was used for the lead foot, which was supported on a 0.051 mm (0.002 inch) thick solder joint on a pad 0.76×1.8 mm (0.030×0.070 inch). For analysis of the initial rapid loading stress, a low strain elastic model for solder was used with modulus 8 GPa (1.16 MPSI).

Normalized steady-state isotherms and solder joint stress contours are shown in Fig. 1(b) and 1(c). The transient response is given in Fig. 2, showing that the maximum solder joint equivalent stress tracks the mean lead frame temperature

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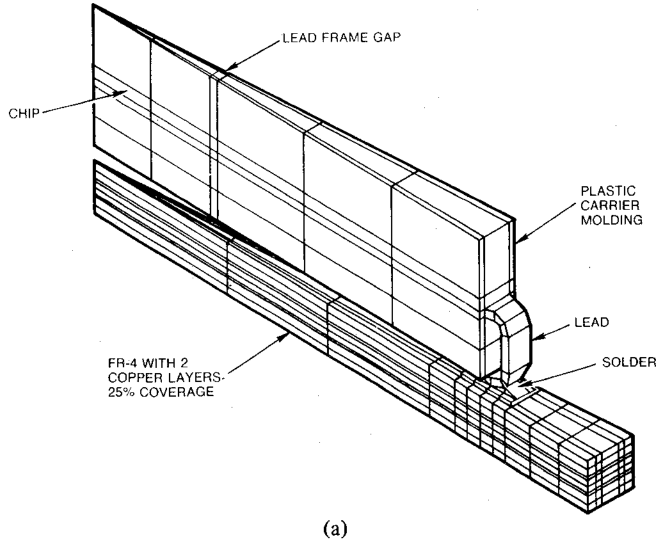
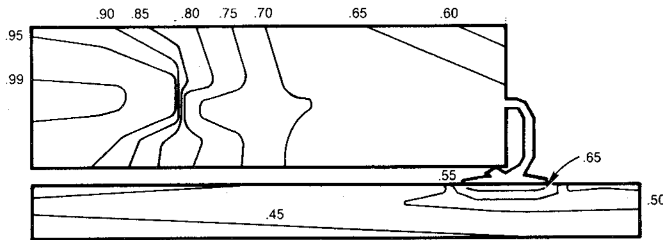
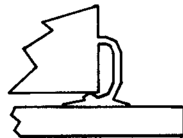


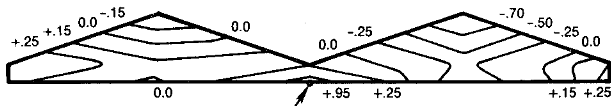
(a)



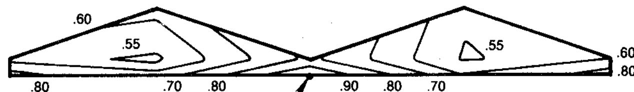
T_{MAX} = 32.3 C (AMBIENT = 0°C)
68 I/0 PLCC ON FR-4
1 WATT TOTAL, 2 M/S FORCED CONVECTION

(b)





PRINCIPAL STRESS Σ_1



EQUIVALENT STRESS Σ_E

$$\Sigma_E = \frac{1}{\sqrt{2}} [(\Sigma_1 - \Sigma_2)^2 + (\Sigma_2 - \Sigma_3)^2 + (\Sigma_3 - \Sigma_1)^2]^{1/2}$$

(c)

Fig. 1. Finite element analysis of surface mounted 68 PLCC solder joint thermal stress. (a) Finite element wedge model. (b) Steady state isotherms. (c) Steady state solder joint stress contours.

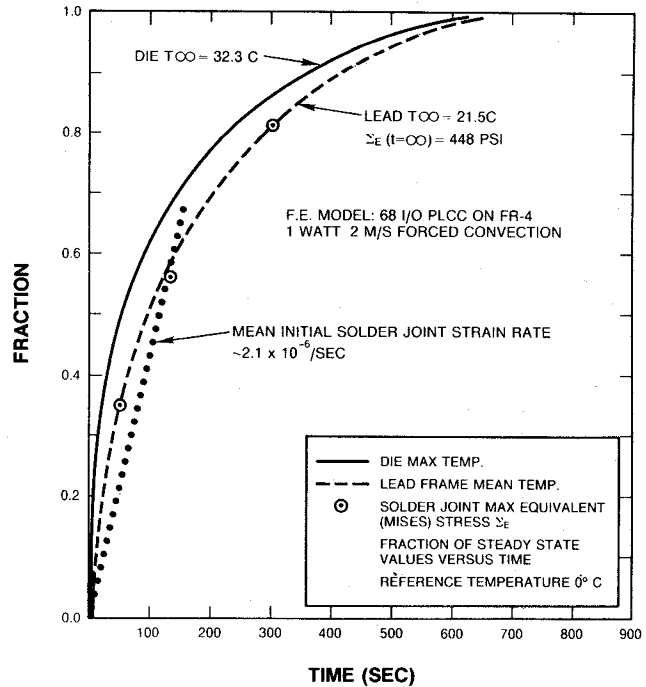


Fig. 2. Thermal and thermal stress transient response on wedge model.

rise, attaining 50 percent of steady state value in about 2 min. On the basis of the elastic model, this relates to a peak strain loading rate for portions of the solder joint at 2.1 ppm/s, with maximum steady state "elastic" strains 0.04 percent or less. It can be seen that average steady state stresses are nominally 2 MPa (300 PSI), before significant creep or stress relaxation occurs. The effective net thermal displacement of the lead top relative to bottom is about 5 μm (0.2 mils) nearly parallel to the pad, producing low stresses in the solder.

The Environment for PLCC Solder Fatigue

From the results of this simple model, one expects the initial quasi-elastic joint strains associated with a surface mounted PLCC with compliant leads to be very low, typically 0.02–0.05 percent, depending on carrier size, lead dimensions, thermal characteristics, and other factors. Larger stresses and strains will certainly occur in corner located leads and are sensitive in general to the conditions of board restraint and component placement in actual modules, as has been discussed elsewhere [22]. However the case analyzed here shows that even very low thermal stresses developed during power excursions are sufficient to cause significant creep in the solder, particularly at the high temperature dwell, leading to accumulation of additional joint strains. At 50–60°C and 2 MPa (300 PSI), the creep rate for eutectic Sn/Pb (63/37) is 0.1–10.0 ppm/s, depending on grain size distribution and impurities, but is 1–2 orders magnitude lower at 25°C [3]–[6].

Creep will continually reduce the driving load imposed by spring tension in the lead; 0.1 percent creep strain in 2 h relieves about 50 percent of the initial net lead deflection due to temperature change. The short duration thermal strain rate due to power steps (2 ppm/s for 2 min) can be typically an order of magnitude greater than the hot dwell creep rate (0.1 ppm/s), which could persist for a few hours.

Thus, allowing for lead tension relief, under a mean load of 2 MPa, the total accumulated solder creep strain in 2 h at 50–60°C, 0.25 ppm/s, would amount to about 0.1 percent in the direction of load. Other larger components of effective creep shear strain could be imposed due to the large joint length/thickness ratio (1.8/0.051 = 35). Evidently the total accumulated creep strain will be several times the nominal elastic strains associated with transient loading. This is quite different from the leadless carrier situation, where large forces due to thermal expansion mismatch cause a rapid plastic deformation of a few percent in the joint, amounting to essentially all of the net displacement.

Consequently, the solder thermal fatigue cycle for a leaded carrier can be pictured as one of rapid introduction of quasi-elastic strains over 1–2 min followed by up to several hours accumulation of additional strain by creep. There is a complex interplay among strain rate, creep, and mean stress, against a background of changing temperature. The mechanisms that might contribute to solder fatigue under these conditions have not been firmly established. It has been observed that grain size tends to increase with temperature or strain cycling, or both, with and without attendant decrease in fatigue life [2], [7], [8], [20]. Cyclic grain boundary migration at less than 0.5 percent reversing strain has been observed in pure lead, and associated with fatigue and recovery effects [9]. DeVore has discussed the correlation of microstructural changes to fatigue properties of several alloys. Creep properties of various solders have been considered in relation to fatigue resistance, with weak or inconsistent correlation, which may have been due to the differing test conditions of strain range and temperature [10], [4].

Available Fatigue Data

The majority of existing work on solder fatigue has focused on relatively large strain, a few percent or more, although the seminal work of Gohn and Ellis [11] and Eckel [12] covered 0.2–1.0 percent strain. Usually, quantitative strain controlled fatigue data are taken in isothermal mechanical tests, for example, the well-cited work of Wild [13]. Shaw and Kelly found that high temperature dwell was an important fatigue accelerator in 95/5 Pb/Sn [14], and heuristic arguments for temperature factors were given by Norris and Landzberg together with a limited amount of data [15]. Engelmaier has given an expression for adjustments to the fatigue exponent for moderate changes in test conditions [1].

The relation between strain-controlled isothermal fatigue and thermal cycle fatigue data needs to be put on firmer ground for both large strains (eg., >1 percent, leadless carriers), and low strains (eg., <1 percent, leaded carriers). In addition, for the leaded carrier situation, the effect of complex strain rate loading needs to be understood in relation to thermally activated damage mechanisms that operate over cyclic reversal of low strain, finite stress, and creep.

Isothermal Mechanical Fatigue Experiments

Differential thermal expansion across a direct solder interconnect joint causes a deformation of the joint. In the case of a "bumped" flip chip, the expansion is symmetrical about the chip center with the shear displacement within the planar array of solder joints proportional to radial distance from the chip center. In the case of leadless chip carrier having a peripherial interconnect array, the shear displacement of the joints is also radially proportional and symmetrical. The similarity between this thermally induced shear displacement and that produced by a pure rotation of the chip or chip carrier about the planar center provides a convenient means of mechanically simulating the effect of thermal expansion mismatch [16]. A precision torsional apparatus described below was used to conduct isothermal shear strain mechanical fatigue tests.

Experimental Apparatus

Fig. 3 shows the torsional apparatus mechanical plant, details of specimen mounting, and the system block diagram. A frameless aerospace torque motor was used as the mechanical power source. The rotor is directly coupled to a chuck which grips the chip or chip carrier. The coupling between the rotor and output shaft incorporates a circular spring diaphram with a central hub for attachment of the output shaft. This bronze phosphor spring diaphram provides axial compliance of about 0.27 gm/mm (0.015 lb/inch) with stiff torque coupling between the rotor and specimen chuck. This compliance is desirable for setup as well as to accommodate thermal expansion occuring during the course of the experiment from slight changes in room temperature. The entire motor is mounted on a damped optical table with vibration isolation mounts.

The fixed base of the specimen is attached to the table with a custom clamp which is supported by a vertical micropositioning stage for fine adjustment during setup and for axial force control. The chip or chip carrier fits snugly into a recess in the chuck where it is bonded with epoxy.

Rotational motion to produce 1–5 percent shear strain ranges are on the order of arc minutes. To accurately measure these displacements, a laser extensiometer was employed. Fig. 3(b) illustrates this technique. A low power HeNe laser beam is collimated and focused into a converging beam which impinges upon an optically flat, reflective surface on the specimen chuck. The converging beam extends to a lateral cell electrooptic position sensor. Rotation of the chuck causes angular deflection of the beam path; the motion of the beam focal point on the face of the sensor is registered electrically.

Fig. 3(c) illustrates the simple proportional inner closed loop which provides rapid command tracking. The source of commands for this loop is determined by the experimental protocol. The feedback position was in all cases computer recorded through a DAC. The universal digital/analog interface employed was an HP 3497A data acquisition unit with installable modules for analog to digital and digital to analog conversion as well as versatile channel selection and data storage capabilities.

Strain control was implemented by using the detected laser beam position to generate an error signal relative to a selectable set limit of angular displacement. Real-time tracking of the error signal within the command loop was used to continually adjust motor torque to maintain torsional oscillation with fixed amplitude.

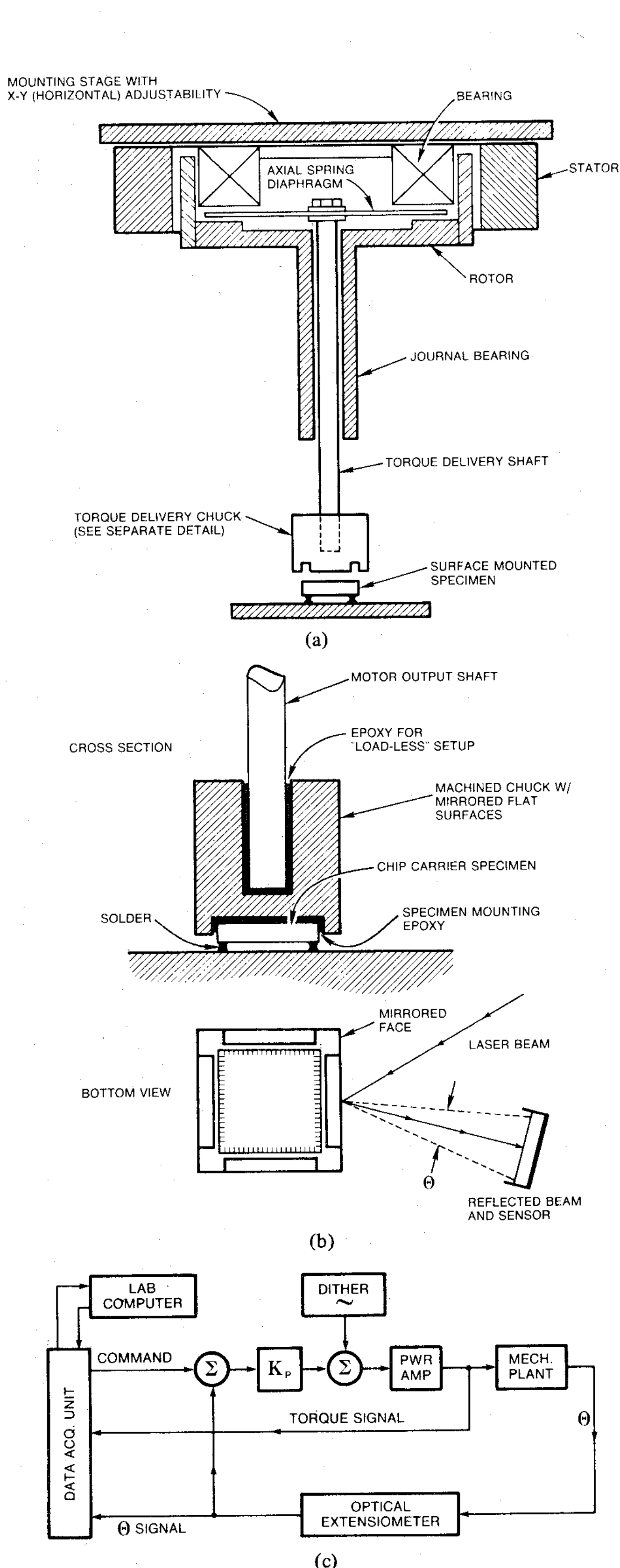


Fig. 3. Torsional apparatus for solder joint isothermal mechanical fatigue. (a) Torque apparatus physical plant. (b) Sample chuck and optics. (c) System block diagram.

Sample Preparation

Both bumped chips and 16 I/O leadless ceramic chip carriers were used as study systems in deference to experimental convenience and precision of solder joint fabrication. Both samples were of comparable size and total joint array torsional compliance, typically 2–4 mrad/N-m.

The 6.6 × 6.6 × 0.6 mm bumped chip was specially constructed for purposes of such tests, and contained 400 bumps of 95/5 Pb/Sn, on a 0.25 mm pitch 20 × 20 rectangular array. The chip was soldered under nitrogen flip-chip style with rosin mildly activated (RMA) type flux to a cofired tungsten–alumina ceramic substrate with matching pad array. After joining of chip and substrate, the nominally cylindrical solder bumps measured 0.15 mm diameter by 0.08 mm height (6 × 3 mils). The rigid ceramic carrier with attached chip was clamped in a rigid fixturing vise. Fig. 3(b) illustrates the set-up.

The 16 I/O ceramic chip carrier, 7.6 × 7.6 mm (0.3 × 0.3 inch), had solder pads approximately 0.64 × 1.0 mm (0.25 × 0.40 inch) of similar construction. These samples were surface mounted to 70 × 70 × 1.6 mm test coupons of ordinary FR-4, using 63/37 Sn/Pb solder paste and vapor phase reflow. Carriers were pretinned by solder pot dipping to remove most of the pad gold flash. The resulting solder joints, defined by the pad dimensions above, had typical heights 0.1 mm (0.004 inch). The assembly was securely clamped with a cutout hold down plate to a rigid stainless steel platform.

Mechanical Fatigue Experiments

A number of strain controlled fatigue experiments were conducted at room temperature (23°C) using bumped chip specimens, at cycle periods of 2, 10, 20, and 40 min. Two types of displacement or strain waveforms were used, a constant strain rate ramp (triangle wave), and a fast loading "square" waveform, shown in Fig. 4 for a 10 min period. Peak motor torque, obtained from the drive voltage, was recorded at each cycle of the test. At fixed strain, this data was proportional to the solder joint array average stiffness. Fig. 5 plots the observed relative stiffness change with number of cycles for several samples at 3.5 percent shear strain. The stiffness, which varies individually, and depends on strain rate, is normalized to the starting initial values. Shown are three typical tests at 2, 10, and 20 min periods with the constant rate ramp wave. Data at the 40 min period are not shown to avoid clutter. Experience showed that the stiffness change was fairly linear below about 80 percent. Table I shows the mean stiffness reduction per cycle in the linear region for these data, which can be reasonably well fit by a relation of the form

$$\text{REDUCTION/CYCLE} = (\text{PERIOD})^{0.45}$$

This is consistent with findings by others concerning the effects of changes in cycling frequency [13], [11], [16]. The linear stiffness reduction per cycle should be inversely related to the number of cycles to failure using mechanical criteria.

A much greater decrease in stiffness per cycle was found when the square wave strain cycle was used, while keeping the

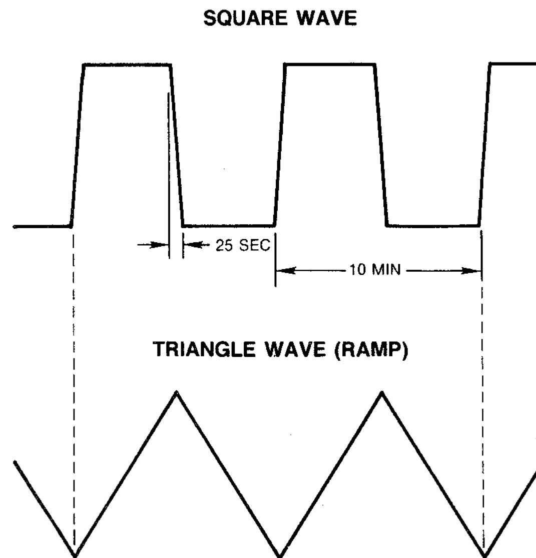


Fig. 4. Strain loading waveforms for mechanical fatigue experiments.

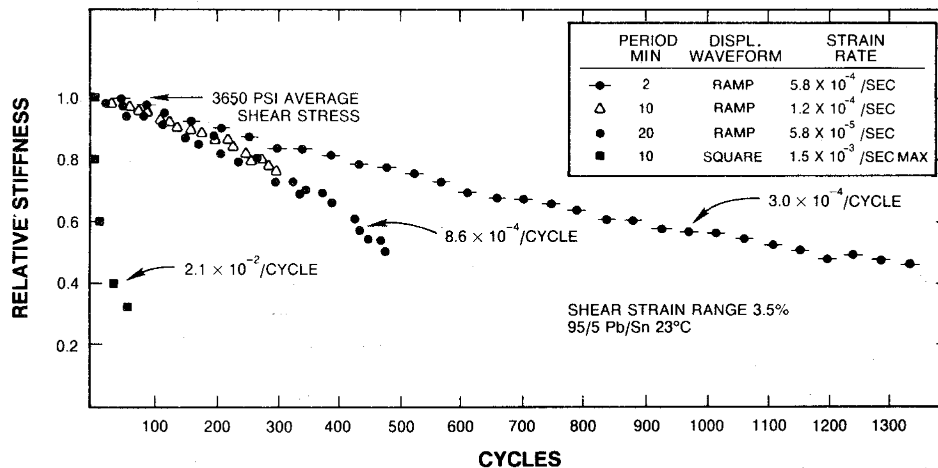


Fig. 5. Isothermal mechanical fatigue data for 95/5 Pb/Sn bumped chip.

TABLE I
FATIGUE DATA 95/5 Pb/Sn AT 23°C, 3.5 PERCENT SHEAR STRAIN

Period (minutes)	2	10	20	40
Reduction/CY $\times 10^{-4}$	3.0	8.6	9.7	13.7

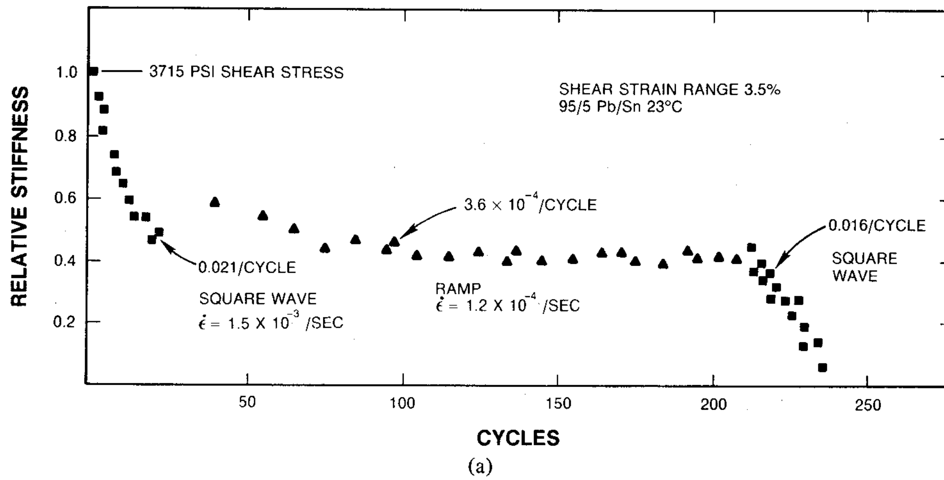
period fixed at 10 min, as indicated in Fig. 5. Fig. 6(a) shows more detail of this experiment, in which the square wave was initially applied for about 30 cycles, causing a net reduction to about 50 percent. Following this, the 10 min ramp was applied at the same strain range, after a 55 h holiday weekend interruption of the test (indicated by a break in the data plot). Upon resumption with ramp cycling, there was a period of 10–20 cycles of settling from a higher stiffness, possibly related to recovery effects, but more probably to the change in strain rate. After this, the reduction per cycle decreased markedly, and remained so for 150 cycles of ramp. Upon reapplication of the square wave with test interruption of a few minutes, the reduction rate again increased markedly. At about 5 percent initial stiffness, the solder failed.

The effects of waveform were also investigated for 63/37 Sn/Pb solder, using the chip carrier specimen. Data from this test are shown in Fig. 6(b). Again, the per cycle decrease in stiffness was found to be much greater with the square wave than the ramp. The square wave was not reapplied after ramp cycling due to accidental breakage of the sample on restart.

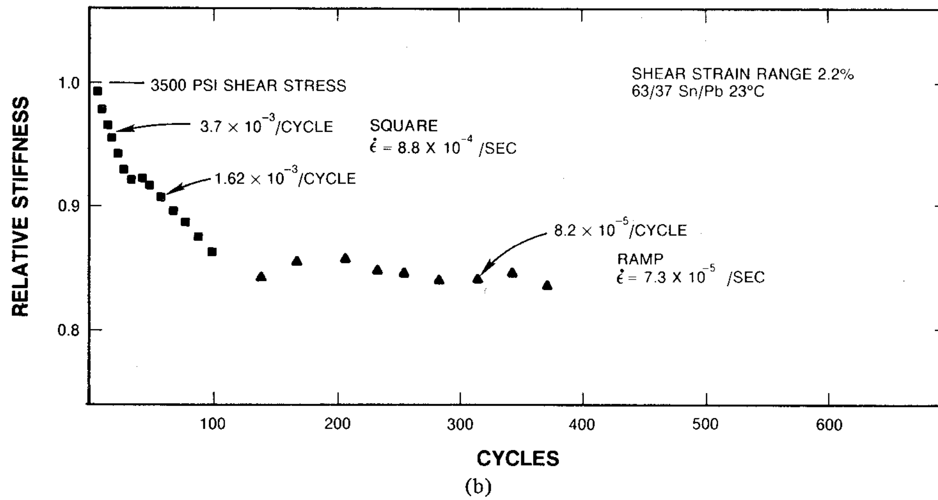
Stress relaxation during the hold portion of the square wave was observed with both solder types, as shown by the example in Fig. 7 for 63/37. Following the fast strain rate load, the stress relaxes for the duration of the hold portion of the cycle to about 64 percent of the peak value.

THERMAL CYCLE FATIGUE EXPERIMENTS

To investigate frequency and strain range effects on fatigue in thermal cycling, a forced air impingement apparatus was used to temperature cycle test specimens between 30–110°C at periods of 2–120 min. The set-up is illustrated in Fig. 8. Specimens were prepared by surface mounting conventional 29 × 29 mm 84 I/O ceramic leadless chip carriers to 80 × 80 mm substrates of several varieties: zinc, aluminum, and type 410 stainless steel. Thermal expansion coefficients of these



(a)



(b)

Fig. 6. Effect of strain waveform on mechanical fatigue rates. (a) Bumped chip data—95/5 Pb/Sn, 3.5 percent strain range. (b) 16 I/O carrier data—63/37 Sn/Pb, 2.2 percent strain range.

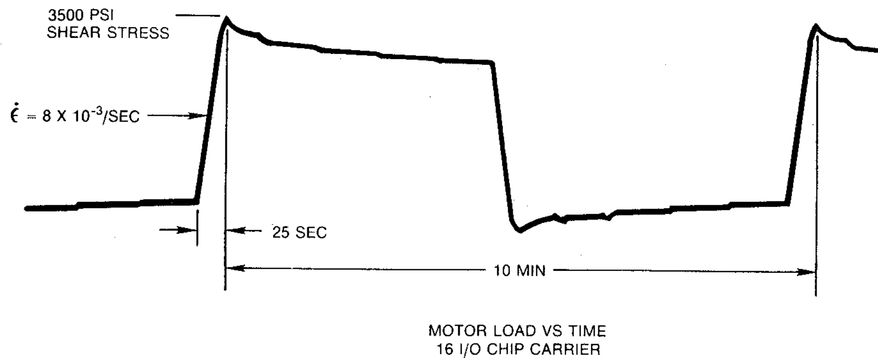


Fig. 7. Room temperature mean solder joint stress relaxation (63/37 Sn/Pb 23°C).

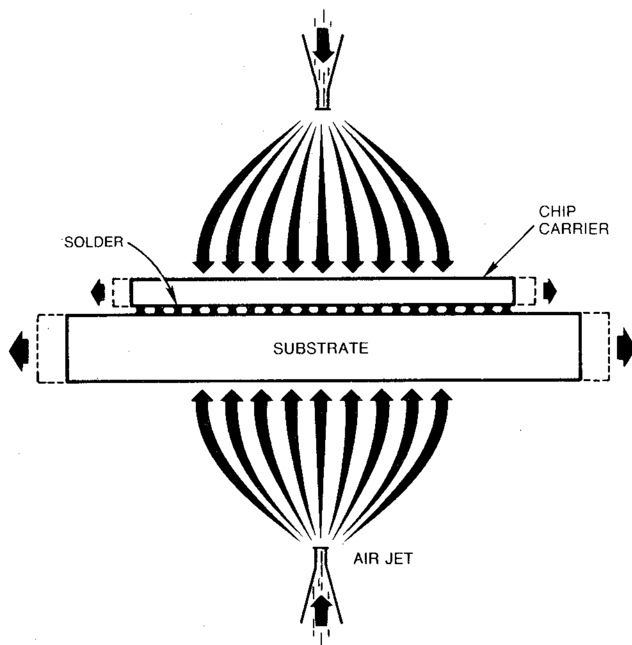


Fig. 8. Illustration of impingement air thermal cycler.

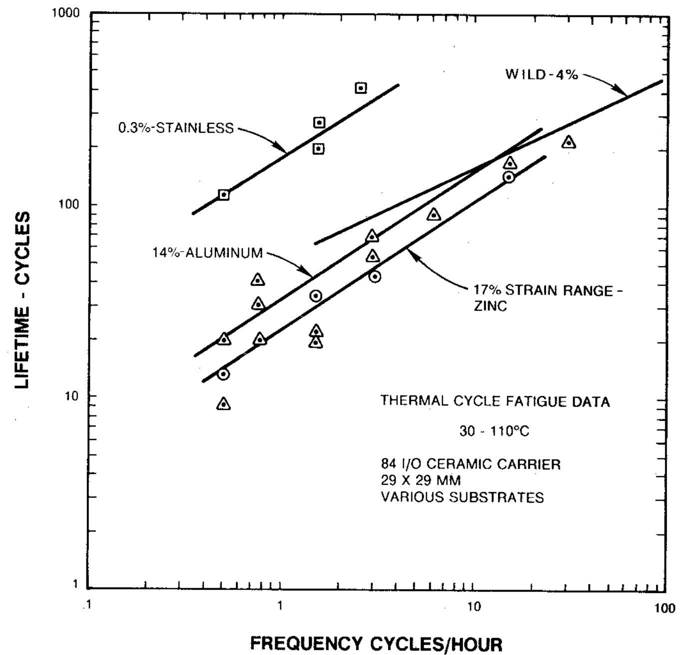


Fig. 9. Thermal cycle fatigue data.

materials were taken as 28, 24, and 9.9 ppm/°C, respectively, for the metals, and 6.5–7.0 ppm/°C for the ceramic. Soldering was accomplished by a typical vapor phase reflow of screened solder paste. Measured joint heights together with relevant mechanical data were used to compute the mean thermal shear strain range of the solder joints, allowing for bending of the carrier and substrate. Failures were counted as 25 percent crack width visible under 70× magnification.

Thermal fatigue data of these experiments are shown in Fig. 9. For purposes of comparison with published data on isothermal fatigue, a liberal interpretation of some of Wild's data is also shown in Fig. 9, with adjustments made for the differences in fatigue criteria [13]. Wild's data show an increasing divergence between lifetime data obtained using observable crack versus electrical resistance criteria. The crack defined failures show an increasingly early onset relative to electrical resistance failures as the strain range is decreased. The crack-resistance offset at 4 percent, the lowest strain range for which both data are shown, was applied to strain and frequency interpolated data of [13, Table IV]. A power law dependence on frequency was assumed. The comparison of fatigue lifetime data obtained with differing failure criteria is tenuous, but it may be useful to compare such data for trends, if not absolute magnitude.

The data of Fig. 9 indicate that the decrease in lifetime with lowering frequency seems to be greater in the thermal cycle tests of these experiments compared to isothermal mechanical cycling, although the comparison with Wild's data is indirect. Also, the lifetime data obtained with the stainless steel substrates at approximately 0.3 percent strain range are comparatively quite pessimistic based on the modest increase in lifetime for more than an order of magnitude lower (computed) strain. The present data are partially at variance with other reported findings of Engelmaier [23], yet are partially supported by the data of Lake and Wild [24].

Discussion

Isothermal Fatigue Data

For both the 95/5 and 63/37 solders, the fatigue rate in the fast loading square wave was considerably greater than during the constant strain rate ramp, at fixed strain range. It appears that the damage acceleration correlates in part with the increased strain rate during the loading portion of the fixed period. Thus, for a 12.1× increase in peak strain rate, the fatigue rate of the 95/5 sample (Fig. 6(a)) increased 56×, and for the 63/37 sample (Fig. 6(b)), 19.5×, for a fixed 10 min period. However the peak strain rate in the 10 min square wave is only 2.6 times the strain rate in the 2 min ramp, yet the fatigue acceleration is 67×.

This suggests that events during the hold period following rapid loading are contributing significantly to fatigue. During this period, significant stress relaxation takes place, as indicated by Fig. 7. Becker found similar acceleration in unidirectional fatigue relaxation time tests, though these were not strain controlled [17]. The strong temperature dependence of solder creep, stress relaxation, ductility, etc., indicate that temperature effects on these findings could be considerable, even to the point of inversion (see, for example, [18], [21]).

Thermal Fatigue Data

Thermal cycle data in Fig. 9 point to two effects warranting further work: 1) the frequency dependence in thermal cycling may be stronger than for isothermal fatigue, as can be seen by comparison with the Wild data; 2) the increase in lifetime with decreasing strain may be much weaker at very low strains. More data are required to complete the picture here, but the present results are not completely at variance with other work, which for the most part do not straddle the 1 percent strain regime. Application of Manson–Halford strain range partitioning to solder at low strain and low frequency thermal cycling

has been used to show that accumulated creep per cycle may accelerate fatigue under these conditions [19].

SUMMARY

Analysis has shown that solder joint stress loading in the leaded carrier is sufficient to cause significant creep under operational conditions. Transient thermal strain rate loading is typically an order of magnitude greater than the subsequent creep rate at low level stress, yet contributes a smaller portion of the total integrated strain.

A sensitive experimental technique for examining solder fatigue through compliance changes has been developed. Comparison with available isothermal mechanical fatigue data is good.

It has been found that rapid strain loading followed by a stress relaxation hold period is much more damaging in fatigue than constant strain rate loading and unloading. Present results are for 23 C, 2–4 percent shear strain.

Thermal cycle fatigue data covering 0.3–17 percent shear strain, 2–120 min period, show stronger frequency dependence than isothermal fatigue data. A diminishing lifetime improvement was indicated for strains less than 1 percent in thermal cycling.

CONCLUSION

Lifetime estimations and fatigue acceleration test design for low strain leaded carrier systems must consider the effects of complex strain and temperature loading on test results and extrapolations. Transient thermal strain rates during loading are typically 10× the subsequent creep rate at low stress. The experimental data presented here suggest that both transient loading and integrated creep strains during stress relaxation must be considered in estimating fatigue damage.

Further work is required to discover the details of the dependence of fatigue on strain loading history and temperature, and the magnitude of such effects at strains less than 1 percent.

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REFERENCES

[1] W. Engelmaier, "Fatigue life of leadless chip carrier solder joints during power cycling," *IEEE Components, Hybrids, Manuf. Technol.*, vol. CHMT-6, no. 3, pp. 232–236, Sep. 1983.

[2] J. K. Hagge, "Predicting fatigue life of leadless chip carriers using Manson-Coffin equations," *Proc. IEPS*, pp. 199–208, 1982.

[3] B. P. Kashyap and G. S. Murty, "Experimental constitutive relations for the high temperature deformation of a Pb-Sn eutectic alloy," *Mater. Sci. Eng.*, vol. 50, pp. 205–213, 1981.

[4] M. B. Shamash, "Development of highly reliable soldered joints for printed circuit boards," Westinghouse Defense and Space Center, Baltimore, MD, Rep. NTIS N69-25697, 1968.

[5] P. A. Ainsworth, "The formation and properties of soft soldered joints," Int. Tin Research Institute, reprinted in *Metals and Materials*, pp. 374–379, Nov. 1971.

[6] W. A. Baker, "The creep properties of soft solders and soft soldered joints," *J. Inst. of Metals*, vol. 65, pp. 277–297, 1939.

[7] D. L. Kinser, J. G. Vaughan, and S. M. Graff, "Reliability of soldered joints in thermal cycling environments," *Int. Mic. Elec. Conf.*, pp. 4–7, 1976.

[8] M. M. I. Ahmed and T. G. Langdon, "The effect of grain size on ductility in the superplastic Pb-Sn eutectic," *J. Mater. Sci. Lett.*, vol. 2, pp. 337–340, 1983.

[9] T. G. Langdon and R. C. Gifkins, "Cyclic grain boundary migration during high temperature fatigue—I. Microstructural observations," *Acta. Metall.*, vol. 1, no. 6, pp. 927–938, 1983.

[10] J. A. DeVore, "Fatigue resistance of solders," *NEPCON West*, pp. 409–414, 1982.

[11] G. R. Cohn and W. C. Ellis, "The fatigue test as applied to lead cable sheath," *Proc. ASTM*, vol. 51, pp. 721–744, 1951.

[12] J. F. Eckel, "The influence of frequency on the repeated bending life of acid lead," *Proc. ASTM*, vol. 51, pp. 745–760, 1951.

[13] R. N. Wild, "Some fatigue properties of solders and solder joints," IBM Rep. 74Z000481, also INTERNEPCON, Brighton, England, Oct. 1975.

[14] H. J. Shah and J. H. Kelly, "Effect of dwell time on thermal cycling of the flip-chip joint," *Proc. Int. Hybrid Microelectronics Symp.*, pp. 3.4.1–3.4.6, 1970.

[15] K. C. Norris and Landzberg, "Reliability of controlled collapse interconnections," *IBM J. Res. and Dev.*, vol. 13, no. 3, pp. 266–271, May 1969.

[16] O. P. Schick and R. Fredriks, "A multicycle method for testing torsional fatigue in flip chip solder interconnections by means of electrohydraulic closed loop control and an IBM Device Coupler 7406," IBM Tech. Rep. TR.22.2251, 1978.

[17] G. Becker, "Testing and results related to the mechanical strength of solder joints," Inst. for Interconnecting and Packaging Electronic Circuits, Evanston, IL, IPC Tech. Paper IPC-TP-288, 1979.

[18] L. R. Lichtenberg, "Comparison of environmental thermal cycle tests on reflow soldered assemblies," *Proc. Int. Symp. on Microelectronics*, Dallas, TX, pp. 65–69, 1984.

[19] M. C. Shine, L. R. Fox, and J. W. Sofia, "A strain range partitioning procedure for solder fatigue," *Proc. Int. Elec. Pack. Soc.*, Baltimore, MD, pp. 346–359, 1984.

[20] E. A. Wright and W. M. Wolverton, "The effect of the solder reflow method and joint design on the thermal fatigue life of leadless chip carrier solder joints," *Proc. 34th Elec. Comp. Conf*, New Orleans, pp. 149–155, 1984.

[21] H. S. Rathore, R. C. Yih, and A. R. Edenfeld, "Fatigue behavior of solders used in flip chip technology," *J. Test and Evaluation*, vol. 1, pp. 170–178, May 1973.

[22] L. R. Fox, M. C. Shine, and J. W. Sofia, "Strain rate loading effects in solder fatigue," *NEPCON West*, 1985.

[23] W. Engelmaier, "Functional cycles and surface mounting attachment reliability," Surface Mount Technology, Silver Spring, Int. Soc. Hyb. Microelectronics, ISHM Technical Monograph Series 6984-002, 1984, ch. 4, pp. 87–114.

[24] J. K. Lake and R. N. Wild, "Some factors affecting leadless chip carrier solder joint fatigue life," *28th National SAMPE Symp.*, pp. 1406–1414, Apr. 12–14, 1983.